

**LOW TEMPERATURE FORMATION OF BACKSIDE OHMIC
CONTACTS FOR VERTICAL DEVICES**

FIELD OF THE INVENTION

5 The present invention relates to ohmic contacts to semiconductor materials. In particular, the invention relates to methods of forming ohmic contacts to devices that include a plurality of semiconductor materials.

BACKGROUND OF THE INVENTION

10 In the microelectronics context, circuits are made from the sequential connection of semiconductor devices. Generally speaking, semiconductor devices are operated by, and are used to control, the flow of electric current within specific circuits to accomplish particular tasks. To connect semiconductor devices to one another, appropriate contacts must be made between the semiconductor devices. Because of their high conductivity, the most useful and convenient materials for
15 carrying current from one device to another are metals.

 Such metal contacts should interfere either minimally or preferably not at all with the operation of the device or the current carrying metal. Furthermore, the metal contact must be physically and chemically compatible with the semiconductor material to which it is attached. The types of contact that exhibit these desired
20 characteristics are known as "ohmic contacts".

 An ohmic contact is usually defined as a metal-semiconductor contact that has a negligible contact resistance relative to the bulk or spreading resistance of the semiconductor, Sze, Physics of Semiconductor Devices, Second Edition, 1981, page 304. As further stated therein, an appropriate ohmic contact will not significantly
25 change the performance of the device to which it is attached, and it can supply any required current with a voltage drop that is appropriately small compared with the drop across the active region of the device.

 Ohmic contacts and methods of producing ohmic contacts are known in the art. For example, U.S. Patents 5,409,859 and 5,323,022 to Glass et al. ("Glass
30 patents"), discuss an ohmic contact structure formed of platinum and p-type silicon carbide and a method of making the ohmic structures. L. Spieß et al., "Aluminium Implantation of p-SiC for Ohmic Contacts," Diamond and Related Materials, vol. 6, pp. 1414-1419 (1997); J. Chen et al., "Contact Resistivity of Re, Pt and Ta Films On

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n-type β -SiC: preliminary results," Materials and Science Engineering, B29, pp. 185-189 (1995); and WO 98/37584 also discuss ohmic contacts and SiC.

Although ohmic contacts and methods of making them are known, the known methods for producing ohmic contacts, and especially

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those produced using a silicon carbide substrate, are difficult even when properly conducted.

The problems associated with obtaining ohmic contacts are myriad and cumulative. Limited electrical conductivity of the semiconductor due to low hole or
5 electron concentrations may hinder or even prevent the formation of an ohmic contact. Likewise, poor hole or electron mobility within the semiconductor may hinder or even prevent the formation of an ohmic contact. As discussed in the Glass patents, work function differences between the contact metal and semiconductor may give rise to a potential barrier resulting in a contact exhibiting rectifying (non-ohmic) current flow
10 versus applied voltage. Even between two identical semiconductor materials in intimate contact with greatly differing electron-hole concentrations, a potential barrier (built-in potential) may exist, leading to a rectifying rather than ohmic contact. In the Glass patents, these problems were addressed by inserting a distinct p-type doped SiC layer between the p-type SiC substrate and the contact metal.

15 More difficult problems are encountered when forming ohmic contacts for newer generation gallium and indium based semiconductor devices. The formation of an ohmic contact between a semiconductor and a metal requires the correct alloying of the semiconductor and the contact metal at their interface. Selectively increasing the hole/electron concentration at the semiconductor surface where the ohmic contact
20 metal is deposited is known as an effective means for enhancing the contact process to achieve an ohmic contact. This process is typically achieved through ion implantation, which is well recognized as a selective doping technique in silicon and silicon carbide technologies. However, in the case of silicon carbide, ion implantation is usually performed at elevated temperatures (typically $>600^{\circ}\text{C}$) in order to
25 minimize damage to the silicon carbide crystal lattice. "Activating" the implanted atoms to achieve the desired high carrier concentrations often requires anneal temperatures in excess of 1600°C , often in a silicon over pressure. The equipment required for this ion implantation technique is specialized and expensive.

After the high temperature ion implant and subsequent anneal, the contact
30 metal is deposited on the implanted substrate surface and annealed at temperatures in excess of 900°C . This method of forming contacts on semiconductor devices that

incorporate gallium nitride or indium gallium nitride is not feasible because these compounds disassociate at elevated temperatures.

One theoretical answer to this problem would be to form an ohmic contact on the substrate prior to growing the delicate epitaxial layers (e.g. gallium nitride layers) necessary to complete the semiconductor device. This approach is undesirable, however, because it inserts an undesired contaminant, the contact metal, into the epitaxial growth system. The contaminant metal can effect epitaxial growth by interfering with lattice growth, doping, rate of reaction or all of these factors. In addition, metal impurities can degrade the optical and electrical properties of the epitaxial layers.

Similarly, many semiconductor devices such as metal-oxide-semiconductor field-effect transistors ("MOSFETS") require a layer of a semiconductor oxide (e.g. silicon dioxide). The high temperatures associated with traditional ion implantation techniques and implant or contact metal annealing processes place high stress on oxide layers, which can damage oxide layers, the semiconductor-oxide interface and the device itself. Alternatively, forming the ohmic contact prior to creating the oxide layer is not practical because the oxidizing environment utilized to form the oxide layers has adverse effects on the ohmic contact.

Accordingly, a need exists for a practical and economical method for forming an ohmic contact for use in conjunction with a semiconductor device that does not exhibit the manufacturing problems previously discussed. The need also exists for a type of a semiconductor device that incorporates an ohmic contact but is economic to manufacture.

OBJECT AND SUMMARY OF THE INVENTION

It is an object of the invention is to provide a semiconductor device that incorporates an ohmic contact.

It is a further object of the invention to provide a semiconductor device comprising silicon carbide and an ohmic contact.

It is a further object of the invention to provide a semiconductor device that incorporates an ohmic contact that is economic to manufacture.

It is a further object of the invention to provide a method for forming a

semiconductor device that incorporates an ohmic contact.

The invention meets these objects with a method for forming a metal-semiconductor ohmic contact for a semiconductor device. The method comprises implanting a selected dopant material into a surface of a semiconductor substrate
 5 having an initial conductivity type. The implanted dopant provides the same conductivity type as the semiconductor substrate. The dopant implantation is followed by annealing the implanted semiconductor substrate a first time at a temperature and for a time sufficient to activate the implanted dopant atoms and increase the effective carrier concentrations. Depositing a metal on the implanted
 10 surface of the semiconductor material follows the first anneal. Thereafter, an annealing of the metal and the implanted semiconductor material occurs. This second anneal is at a temperature below which significant degradation of any epitaxial layers placed on the substrate would occur, but high enough to form an ohmic contact between the implanted semiconductor material and the deposited metal.

15 The invention also meets these objects with a semiconductor device comprising a semiconductor substrate having a first surface and a second surface and a first conductivity type. The device also comprises at least one epitaxial layer that is grown or placed upon the first surface of the semiconductor substrate. The semiconductor substrate is further defined as having a zone of increased carrier
 20 concentration in the substrate extending from the second surface (the surface opposite the epitaxial layer) toward the first surface. The device further comprises a layer of metal deposited on the second surface of the substrate to form an ohmic contact at the interface of the metal and the zone of increased carrier concentration.

25 The foregoing and other objects, advantages and features of the invention and the manner in which the same are accomplished, will become more readily apparent upon consideration of the following detailed description of the invention taken in conjunction with the accompanying drawings, which illustrate exemplary embodiments, and wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

30 FIG. 1 is a schematic cross-sectional diagram of a semiconductor device according to the present invention.

DETAILED DESCRIPTION

Referring now to FIG. 1, a schematic of a semiconductor device 10 according to the invention is presented. The device 10 comprises a semiconductor substrate 12, which for purposes of explanation is considered to be SiC. It should be understood, however, that other semiconductor materials, such as silicon, may be used as a

Situated adjacent the SiC substrate 12 are the additional components 14 necessary to complete the semiconductor device. For example and as represented in

15 The claimed device is further characterized as having a zone of increased carrier concentration 16 on the backside of the semiconductor substrate. In other words, the semiconductor substrate, in this case SiC, has a carrier concentration near the surface of the substrate opposite the epitaxial layers that is higher than the carrier concentration exhibited in the remainder of the substrate.

For example and still referring to FIG. 1, a preferred embodiment of the claimed device comprises a n-type SiC substrate doped with nitrogen. It should be understood that n-type SiC formed of other n-type dopants along with the various types of p-type SiC also may be used in accordance with the invention. The SiC

substrate 12 is preferably slightly to highly doped and possess an initial carrier concentration between about 1×10^{15} and about $1 \times 10^{19} \text{ cm}^{-3}$. The terms "slightly" and "highly" are imprecise and are purposely used to show that the initial carrier concentration may vary considerably. Although the initial carrier concentration may vary considerably, testing has shown that substrates that are initially moderate to highly doped provide the best results. Through ion implantation of a selected dopant material (e.g. nitrogen) at the surface opposite the epitaxial layers 14, a zone 16 is created that contains a higher carrier concentration than the remainder of the substrate 12. Preferably, the ion implantation is conducted at a level that creates a zone of increased carrier concentration 16 on the backside of the substrate that exhibits a carrier concentration between about 1×10^{18} and about $1 \times 10^{20} \text{ cm}^{-3}$ and that is always higher than the initial carrier concentration.

Those skilled in the art will recognize that a zone of increased carrier concentration as described previously may also be formed during the growth of the substrate. However, the difficulties associated with the variable feed rates of the required dopants and other difficulties typically associated with crystal growth methods make this approach impractical.

The preferred n-type dopants for use in forming the zone of increased carrier concentration 16 are nitrogen, arsenic and phosphorous. Preferred p-type dopants for use in forming the zone of increased carrier concentration 16 are aluminum, boron and gallium.

Although Applicant does not wish to be bound by a particular theory, evidence suggests that the zone of increased carrier concentration 16 allows for the creation of a metal contact that exhibits ohmic properties. In a preferred embodiment, a selected contact metal 18 having a melting point, vapor pressure and physical and chemical properties suitable for use with the overall semiconductor device is deposited at the surface of the SiC substrate at the zone of increased carrier concentration 16 to form an interface 20 between the metal and the substrate. Preferred metals include nickel, palladium, platinum, aluminum and titanium with nickel being most preferred. The device, including the metal and the substrate is then annealed at a temperature low

enough to avoid damage to the device and specifically any epitaxial layer, but high enough to form an ohmic contact at the interface of the metal and substrate.

Again, although the Applicant does not wish to be bound by any particular theory, it appears useful to create the zone of increased carrier concentration to serve
5 as the receptor for the contact metal. Thus, in another embodiment, the invention comprises the method of forming the ohmic contact utilized in the previously described semiconductor device.

In a broad aspect, the invention is a method for forming a metal-
semiconductor contact for a semiconductor device. The method comprises implanting
10 a selected dopant material into a semiconductor substrate having a first conductivity type and wherein the implanted dopant provides the same conductivity type as the substrate. For purposes of this discussion it will be assumed that the semiconductor substrate is a SiC substrate and that the dopant material is deposited into a surface of the SiC substrate. Those skilled in the art, however, will readily recognize that the
15 invention may be easily adapted for use with other semiconductor materials. An annealing step follows the implanting of the selected dopant material. In this annealing step the implanted SiC substrate is annealed at a temperature and for a time sufficient to activate the implanted dopant atoms to effectively increase the carrier concentration of the implanted dopant atoms in the SiC substrate. A contact metal is
20 then deposited on the implanted surface of the SiC substrate. The deposited contact metal and the implanted surface of the SiC substrate are then annealed. This second annealing is at a temperature below that at which any epitaxial layer placed on the substrate would experience significant degradation but high enough to form an ohmic contact between the implanted SiC and the deposited metal.

25 In a preferred embodiment, the semiconductor substrate may comprise a n-type or p-type substrate that may possess a slight, moderate, or high initial dopant concentration. For example, where n-type SiC is the substrate, the SiC substrate may possess an initial dopant concentration from about 1×10^{15} (slightly doped) to 1×10^{19} cm^{-3} (highly doped). The terms "slight," "moderate," and "high" are imprecise and
30 are used to indicate that the initial concentration of dopant in the substrate material may vary. Testing has shown that moderate to highly doped substrates achieve the

best results with the invention.

The semiconductor substrate is then implanted with a selected dopant material and annealed. Preferably, the dopant implantation occurs at room temperature and the subsequent annealing occurs at a temperature between about 800°C and about 1300°C.

- 5 Dopants usually associated with the conductivity type of the substrate may be used as the dopant for the implantation step. For example, when n-type SiC initially doped with nitrogen is the substrate, nitrogen may serve as the implanted dopant. Likewise, when p-type SiC initially doped with aluminum is the substrate, aluminum may serve as the implanted dopant. Other possible n-type dopants are arsenic and phosphorous.
- 10 Boron and gallium may serve as alternative p-type dopants.

- Those skilled in the art will readily recognize that the implanting of the dopant material may be accomplished at high temperatures. In fact, high temperature implantation is typically preferred in the SiC context in order to reduce damage to the SiC lattice structure. In the SiC context, however, high temperature ion implantation
- 15 places constraints on the commercial use of the invention. Ion implanting equipment with the capability of heating the SiC substrate during implantation are atypical, expensive and intended for research and development rather than low cost, high volume applications. Furthermore, when SiC substrates are heated to high temperatures, they must be heated and cooled at a rate that will not produce fractures
- 20 thereby slowing down the production process.

- Accordingly, room temperature implantation is the preferred implantation method for use in the invention. It has been discovered that room temperature implanting of dopant followed by an annealing step in a simple vented furnace capable of reaching 1300°C and holding 100 or more substrate wafers achieves
- 25 satisfactory results and greatly increases throughput.

- The room temperature implantation of dopant is preferably conducted so as to create a zone of increased dopant concentration near the implanted surface of the semiconductor substrate. FIG. 2 is a schematic representation of the implantation process according to the invention. In this example, a n-type SiC substrate **22** having
- 30 an initial dopant concentration of approximately $1 \times 10^{18} \text{ cm}^{-3}$ is implanted with atomic or diatomic nitrogen **24** at energies of 10 to 60 keV with doses of $1 \times 10^{13} \text{ cm}^{-2}$ or more.

In some instances more than one implant energy may be used to create a more graduated carrier concentration distribution. The implantation process produces a zone 26 near the implanted surface of the SiC substrate approximately 1000 angstroms in depth having a total chemical dopant concentration of approximately
5 1×10^{19} to $1 \times 10^{20} \text{ cm}^{-3}$ with the concentration of the implanted dopant decreasing as the distance from the implanted surface increases. The dopant concentration outside of the zone of increased dopant concentration 26 remains substantially the same as the initial dopant concentration. The boundary of the zone of increased carrier concentration 26 is represented as a dotted line to indicate that the change in carrier
10 concentration between the zone 26 and the remainder of the substrate is not distinct but gradual. Those skilled in the art should recognize that the implantation energy or the dose may be readily changed to achieve desired concentrations and thicknesses.

As mentioned previously, it is necessary to anneal the implanted substrate. The annealing is required because some of the implanted dopant ions are not "active"
15 immediately after implantation. The term "active" is used to describe the availability of the implanted ions to contribute to the overall carrier concentration of the implanted substrate.

During implantation, the crystal lattice of the SiC substrate is essentially bombarded by dopant ions. These ions crash into the crystal lattice where they are
20 retained. This bombardment does not result in a perfect insertion of dopant ions into the existing crystal lattice. The initial positioning of many of the dopant ions may prevent the ions from being "active" participants in the crystal lattice, which itself may be damaged by the bombardment. Annealing (*i.e.*, heating) the implanted SiC substrate provides a mechanism by which the implanted ions and the crystal lattice of
25 the substrate may rearrange in a more orderly fashion and recover from the damage incurred during the dopant implantation.

Using round numbers solely for explanatory purposes, the implanting process may be thought of as follows. If 100 nitrogen ions are implanted in an n-type SiC substrate having an initial concentration of x nitrogen atoms, immediately after
30 implantation the substrate may only exhibit the characteristics associated with a substrate having "x+10" nitrogen ions. However, if the substrate is then annealed and

25 Preferably, the contact metal is deposited on the substrate surface to form a layer 300 angstroms thick or more. The deposition is followed by a second anneal. This anneal, however, is not a high temperature long duration anneal. This anneal preferably occurs at a temperature less than about 1000 ° C and most preferably less than about 800°C for 20 minutes or less and most preferably for 5 minutes or less.

30 These temperatures and time periods are sufficiently low to avoid damaging any epitaxial layers that are on the substrate. The annealing of the contact metal to the

semiconductor substrate results in an ohmic contact at the interface of the metal and substrate.

In a more specific embodiment of the invention, a metal semiconductor according to the invention was created using a n-type SiC substrate which was first
5 implanted at an energy of 50 keV with a $3 \times 10^{14} \text{ cm}^{-2}$ dose of atomic nitrogen followed a second implantation at 25 keV at $5 \times 10^{14} \text{ cm}^{-2}$. The implantation was followed by an activation anneal at 1300 °C for 60 to 90 minutes in an argon ambient in a furnace. Subsequently, the contact metal, nickel was deposited on the implanted surface at a thickness of 2500 Angstroms. The contact anneal was then performed at 800 °C for 2
10 minutes in argon. The resulting ohmic contact exhibited satisfactory ohmic properties.

Those skilled in the art should recognize that it is also possible to conduct the contact anneal in situ with epitaxial growth.

The invention offers a substantial advantage for vertical devices such as
15 photodetectors, light emitting diodes (LEDs), lasers, power devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), pn junctions and Schottky rectifiers, and microwave devices such as SITs (static induction transistors). In the case of detectors, LEDs and lasers, epitaxially grown gallium nitride and indium gallium nitride layers are not to be
20 subjected to anneals at temperatures that would severely damage the layers. In the case of indium gallium nitride, time at elevated temperatures becomes more critical as the indium composition of the alloy increases. Reducing the backside contact anneal temperature also reduces the potential for cracking in or disassociation of indium or gallium components in the strained heteroepitaxial films grown on SiC substrates.

25 In the case of power devices where homoepitaxial films of SiC are grown on the substrate and thermally grown or thermally regrown (reoxidized or annealed), oxides have an integral role in the device performance and a lower anneal temperature is an advantage. The backside metal contact can not be subjected to the oxidizing ambient that is required to grow the SiC-silicon dioxide interface, therefore, the
30 backside ohmic contact must be deposited and annealed after the silicon dioxide is grown (reoxidized or regrown). Unfortunately, prior art anneal temperatures of about

850 °C or greater are required to subsequently form a contact to the back of the substrate (more typically 900 to 1050 °C) will create defects at the SiC-silicon dioxide interface due to mismatches in the rate of thermal expansion. This is particularly bad for MOSFETs and IGBTs.

5 SiC technology is in its infancy and many proposed devices and material structures are yet to be examined or developed. Further development of this process may lead to anneal temperatures that are even lower, ultimately leading to an ohmic contact between the metal and the semiconductor as deposited (*i.e.*, no anneal).

10 The invention has been described in detail, with reference to certain preferred embodiments, in order to enable the reader to practice the invention without undue experimentation. However, a person having ordinary skill in the art will readily recognize that many of the components and parameters may be varied or modified to a certain extent without departing from the scope and spirit of the invention. Furthermore, titles, headings, or the like are provided to enhance the reader's
15 comprehension of this document, and should not be read as limiting the scope of the present invention. Accordingly, only the following claims and reasonable extensions and equivalents define the intellectual property rights to the invention.